REMARKS

Objections to the Specification

The Specification has been amended to address these objections. The amendments repeat matter already included in the Specification and correct a typographical error. Accordingly, the amendments present no new matter.

Objections to Drawings

Proposed amended drawings are included herein. Changes are indicated by red ink. The drawings have been amended to include item 38 and a pointing line for item 26. These items are referred to the Specification on page 2, line 22 to page 3 line 2. Accordingly, these changes present no new matter.

Rejections Under 35 U.S.C. §112, Second Paragraph.

Claim 6 has been cancelled.

Rejection of Claims 1-6 Under 35 U.S.C. §102(a) based on Applicant's Background Art (*Background Art*).

The invention of amended claim 1 is directed to a semiconductor device with a device structure having an insulating film formed from gas containing carbon and including a contact, a gate electrode, and a silicon nitride film. The contact penetrates an interlayer insulating film and is electrically connected with a diffusion layer in a silicon substrate. The gate electrode is formed on the silicon substrate and contains a nitride film at upper and side portions. The silicon nitride film is formed on the silicon substrate while traversing a region except a portion for providing the electrical connection between the contact and the diffusion layer and formed on the nitride film at the upper and side portion of the gate electrode.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference. Because the *Background Art* does not show all elements of claim 1, this ground of rejection is traversed.

The *Background Art* shows a gate electrode containing silicon nitride films. However, such silicon nitride films are not formed on the nitride film at the upper and side portion of a gate

electrode, as recited in claim 1. Instead, the *Background Art* shows one nitride layer formed on the top of a gate electrode, and another nitride layer formed on the side of a gate electrode.[1]

For these reasons the rejection of claim 1 and 2 is traversed.

Applicant has amended the claims to include new claims 21-24, which are believed to be allowable over the *Background Art*.

The semiconductor device of new claim 21 includes a device structure including an insulating film formed from gas containing carbon and including a contact, a capacitor contact, a conductor, and a silicon nitride film. The contact penetrates a first interlayer insulating film and is electrically connected with a diffusion layer in a silicon substrate. The capacitor contact is interposed between a lower electrode of a memory cell capacitor and the contact while penetrating a second interlayer insulating film and a third interlayer insulating film. The conductor is formed on the second interlayer insulating film and contains a nitride film at upper and side portions. The silicon nitride film is formed on the third interlayer insulating film while traversing a region except a connection portion between the lower electrode and the capacitor contact and is formed above the nitride film at the upper portion of the conductor.

The *Background Art* shows a bit line containing a nitride film at upper and side portions.[2] However, neither nitride film of the *Background Art is* is formed above a nitride film formed at the upper portion of the conductor.[3]

New claim 22 depends from new claim 21, which is believed to be allowable.

The semiconductor device of new claim 23 includes a device structure including an insulating film formed from gas containing carbon and including a contact, a conductor, and a silicon nitride film. The contact is electrically connected with a diffusion layer formed in the silicon substrate while penetrating a first interlayer insulating film. The contact is electrically connected to a capacitor contact that is interposed between a lower electrode of a memory cell

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[1] See the Specification, FIG. 16(a), which shows a gate electrode **22** that includes silicon nitride film **20** on the top of a gate electrode **18/16**, and silicon nitride film **24** on the side of the gate electrode **18/16**.

[2] See the Specification, FIG. 17, which shows a bit line **38** which includes nitride films (**40** and **36**).

[3] See the Specification, FIG. 17, which shows nitride layer **36**, which is not formed above any other nitride film, let alone a nitride film at an upper portion of a conductor. Similarly, nitride layer **40** is not formed above any other nitride layer.

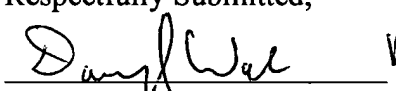
capacitor and the contact while penetrating a second interlayer insulating film and a third interlayer insulating film for providing an electrical connection between the lower electrode and the contact. The conductor is formed on the second interlayer insulating film and contains a nitride film at upper and side portions. The silicon nitride film is formed between the second and third interlayer insulating film while traversing a region except a connection portion between the lower electrode and the capacitor contact and is formed on the nitride film at the upper and side portions of the conductor.

As noted above, the *Background Art* shows a bit line containing a nitride film at upper and side portions. However, neither such nitride layer of the *Background Art* is formed on the nitride film at the upper and side portions of the conductor. Applicant incorporates the comments set forth above for claim 1 to address this ground of rejection.

For all of these reasons, Applicant's believe that the newly submitted claims are allowable over the *Background Art.*

Claims 1 and 2 have been amended. Claims 3-6 have been cancelled. Claims 21 to 24 have been added. The present claims 1, 2 and 21-24 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,



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Version With Markings to Show Changes Made

In the Specification.

Please insert the following paragraph beginning on page 12, line 8.

FIG. 4 is a cross-sectional view of a portion of a DRAM after various processing steps according to an embodiment.

Please replace the paragraph beginning on page 2, line 15 with the following.

A first interlayer insulating film **26** is formed on word line **22**. A cell contact hole is formed between word lines **22** to expose the silicon substrate **12** through first interlayer insulating film **26**. Cell contact hole is filled with an electrically conductive material such as DOPOS and tungsten (W) to form a cell **[contract] contact** plug **30**.

In the Claims.

1. (Amended) A semiconductor device on a silicon substrate, having a device structure including an insulating film formed from gas containing carbon, comprising:

a contact which penetrates an interlayer insulating film and is electrically connected with a diffusion layer in the silicon substrate;

a gate electrode which is formed on the silicon substrate and contains a nitride film at upper and side portions;

a silicon nitride film **for preventing carbon diffusion, which is formed on the silicon substrate while traversing a region except a portion for providing the electrical connection between the contact and the diffusion layer, and is formed on the nitride film at the upper and side portions of the gate electrode [formed between the insulating film and the silicon substrate for preventing carbon from diffusing to the silicon substrate].**

2. (Amended) The semiconductor device according to claim 1, wherein:

the insulating film includes tantalum oxide (Ta_2O_5)**; and**

the semiconductor device is a dynamic random access memory having a memory cell capacitor film including the tantalum oxide.

Please cancel claims 3 to 6.

21. (New) **A semiconductor device on a silicon substrate, having a device structure including an insulating film formed from gas containing carbon, comprising:**

a contact which penetrates a first interlayer insulating film and is electrically connected with a diffusion layer in the silicon substrate;

a capacitor contact that is interposed between a lower electrode of a memory cell capacitor and the contact while penetrating a second interlayer insulating film and a third interlayer insulating film;

a conductor which is formed on the second interlayer insulating film and contains a nitride film at upper and side portions;

a silicon nitride film for preventing carbon diffusion, which is formed on the third interlayer insulating film while traversing a region except a connection portion between the lower electrode and the capacitor contact, and is formed above the nitride film at the upper portion of the conductor.

22. (New) The semiconductor device according to claim 21, wherein:

the insulating film includes tantalum oxide (Ta_2O_5); and

the semiconductor device is a dynamic random access memory having a memory cell capacitor film including the tantalum oxide.

23. (New) A semiconductor device on a silicon substrate, having a device structure including an insulating film formed from gas containing carbon, comprising:

a contact that is electrically connected with a diffusion layer formed in the silicon substrate while penetrating a first interlayer insulating film, the contact is electrically connected to a capacitor contact that is interposed between a lower electrode of a memory cell capacitor and the contact while penetrating a second interlayer insulating film and a third interlayer insulating film for providing an electrical connection between the lower electrode and the contact;

a conductor which is formed on the second interlayer insulating film and contains a nitride film at upper and side portions;

a silicon nitride film for preventing carbon diffusion, which is formed between the second and third interlayer insulating while traversing a region except a connection portion between the lower electrode and the capacitor contact, and is formed on the nitride film at the upper and side portions of the conductor.

24. (New) The semiconductor device according to claim 23, wherein:

the insulating film includes tantalum oxide (Ta_2O_5); and

the semiconductor device is a dynamic random access memory having a memory cell capacitor film including the tantalum oxide.

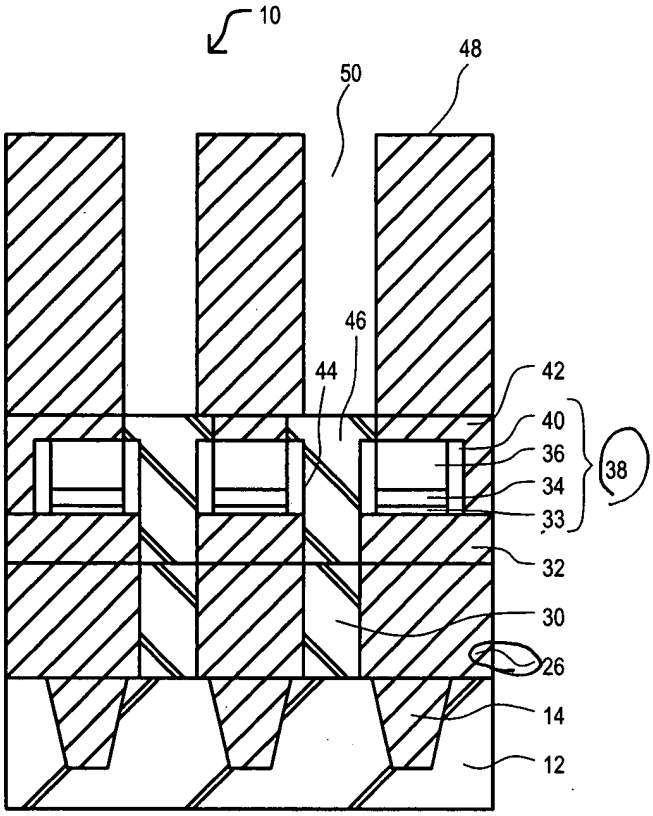

FIG. 17 (BACKGROUND ART)